

ZZZ
PCB DAZ@
DA8900YX000
PCB 125 LA-A792P REV0 M/B 3

S1
FRAME
ECOMV000200

S2
FRAME
ECOMV000200
for GLONASS
@

Compal Confidential

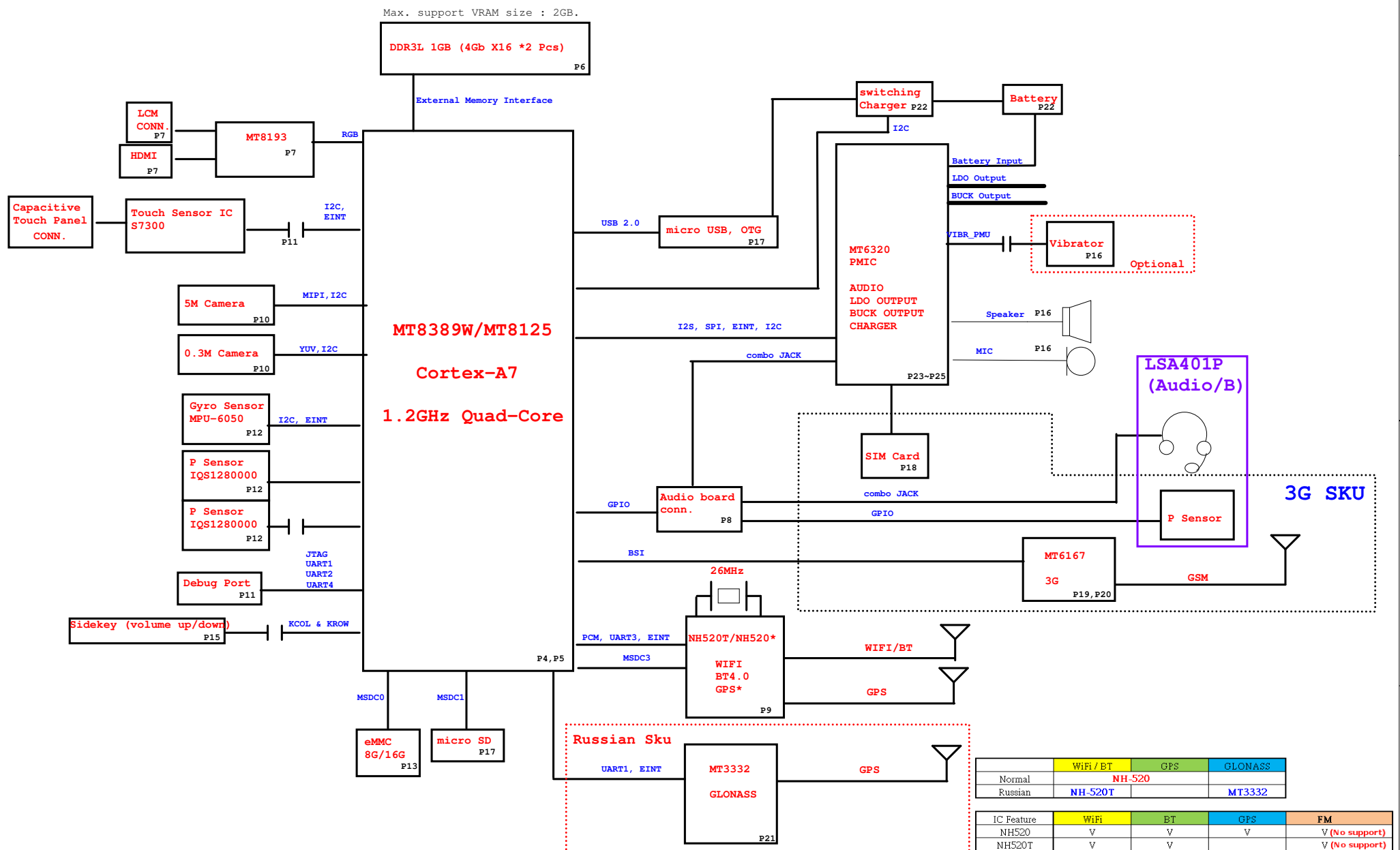
Schematics Document

ZEJ20
LA-A792

2013-08-01
REV: 0.2

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Issued Date	2012/11/09	Deciphered Date	2014/11/09	Title	Cover Page
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ZEJ20 (ZARA 3G) block diagram



	WiFi / BT	GPS	GLONASS
Normal	NH-520		
Russian	NH-520T		MT3332

IC Feature	WiFi	BT	GPS	FM
NH520	V	V	V	V (No support)
NH520T	V	V	V	V (No support)

Voltage Rails

MT6320 Power Plane	Function	Power Level	IDLE	Sleep mode
VCORE_PMU	VCORE switching output	0.75 ~ 1.3	ON	Low voltage
VPROC_PMU	VPROC switching output	0.75 ~ 1.3	ON	Low voltage
VTCXO_1_PMU	LDO output for TCXO	2.8V	ON	OFF
VCAMA_PMU	LDO output for camaera analog	2.8V	ON	Gating by SW
VSRAM_PMU	LDO output used for 1.2V SRAM	1.2V	ON	Low voltage
VDD28_6583	LDO output used for 2.8V IO	2.8V	ON	Gating by SW
VGP2_PMU	LDO output for camaera 1.8V	1.8V	ON	Gating by SW
VEMC_3V3_PMU	LDO output for eMMC&P-sensor	3.3V	ON	Gating by SW
VMCH_PMU	LDO output for SD card	3.3V	ON	Gating by SW
VGP5_PMU	LDO output for Touch panel	2.8V	ON	Gating by SW
DDR3VCCIO	LDO output for DDR3L	1.35V	ON	Gating by SW
VDD33_6583	LCD & Bridge power	3.3V	ON	Gating by SW
VDD18_6583	LDO output used for 1.8V IO	1.8V	ON	Gating by SW
VRF18_PMU	LDO output for RF_MT6167	1.8V	ON	Gating by SW

Main board ID

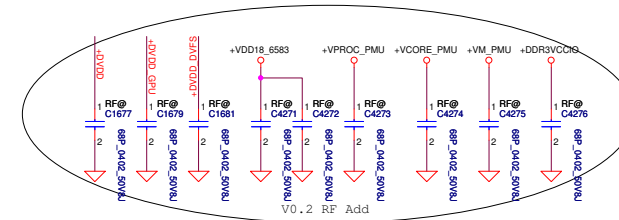
MB_ID0	MB_ID1	
0	X	NH520
0	X	NH520
1	X	Glonass +NH520T
1	X	Glonass +NH520T

I2C address

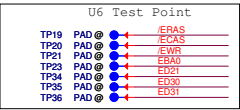
Device	Address(7 bit)	Address(8bit)	
		Write	Read
Gyro+G (MPU-6050)	0x68	0xD0	0xD1
Touch screen (S7300B)	0x20	0x40	0x41
Camera 0.3M	0x21	0x42	0x43
Camera 5M	0x36	0x6C	0x6D
Charge (BQ24196)	0x6B	0xD6	0xD7
PMU(MT6320)			
Battery	0x55	0xAA	0xAB

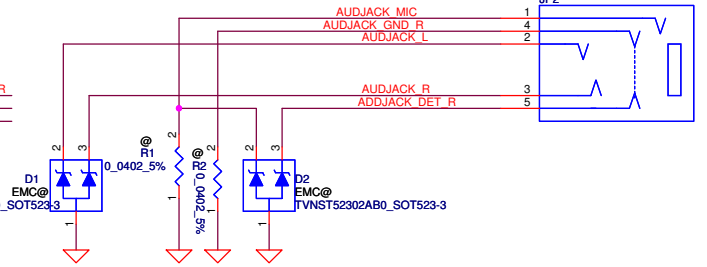
BOM structure

Name	Function	
3G@	3G only	
WIFI_ONLY@	WIFI ONLY	
DAZ@	PCB	
EMC@	for EMC request	
NH520@	AW-NH520	
NH520_EMC@	GPS EMC	
GLONASS@	MT3332	

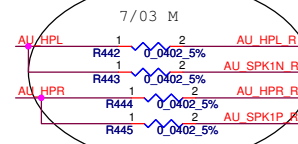
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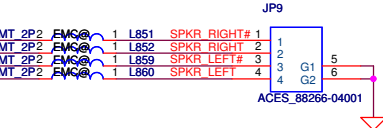
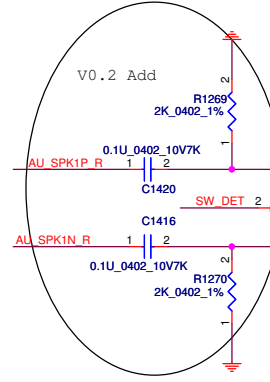


Single via to GND plane



IN	NC to COM COM to NC	NO to COM COM to NO	
L	ON	OFF	HP
H	OFF	ON	SPK

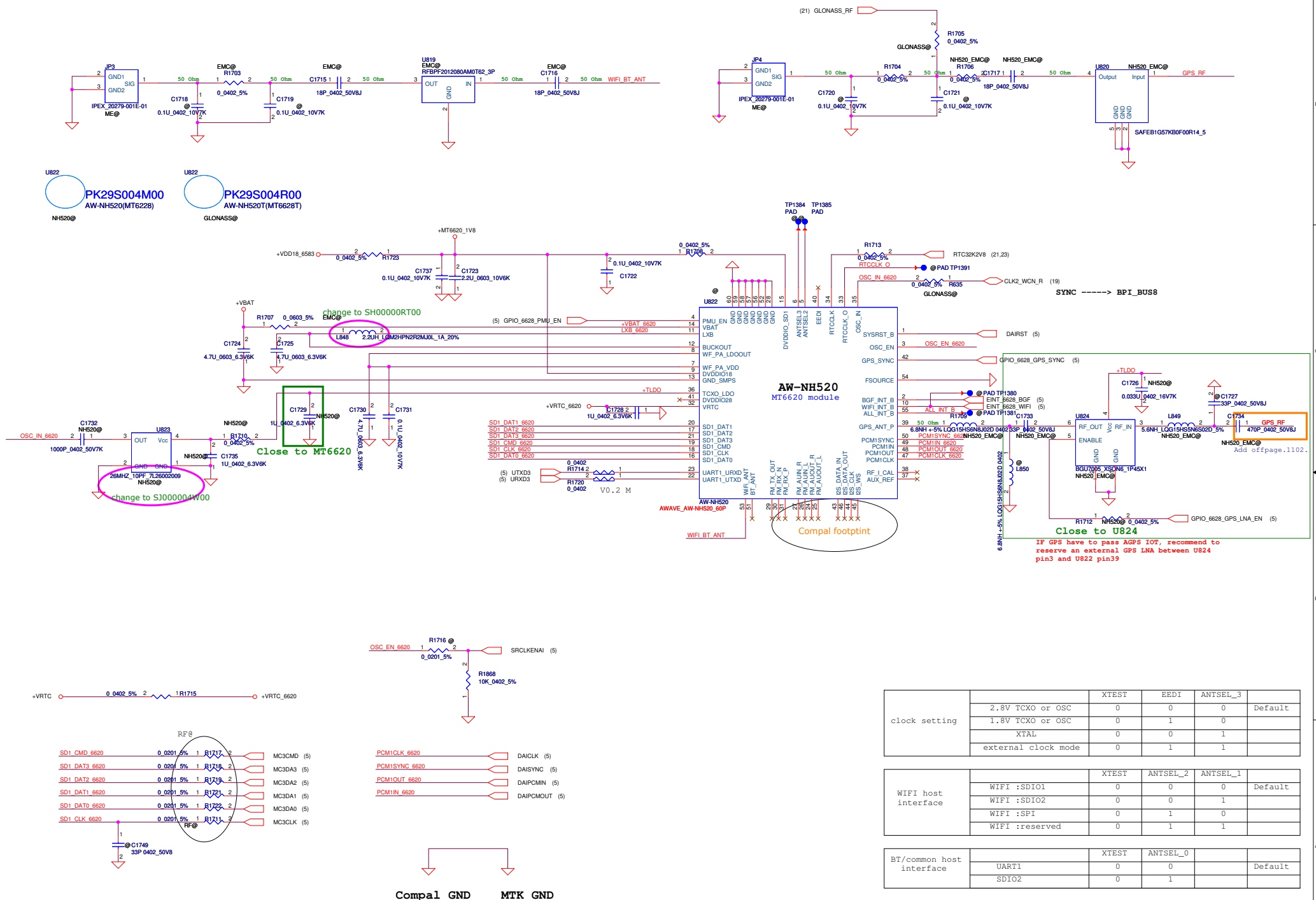
6/7 R1698->R1730
R1697->R1729



GAIN1	GAIN2	
0	0	11d
1	0	14d
0	1	19d
1	1	25d

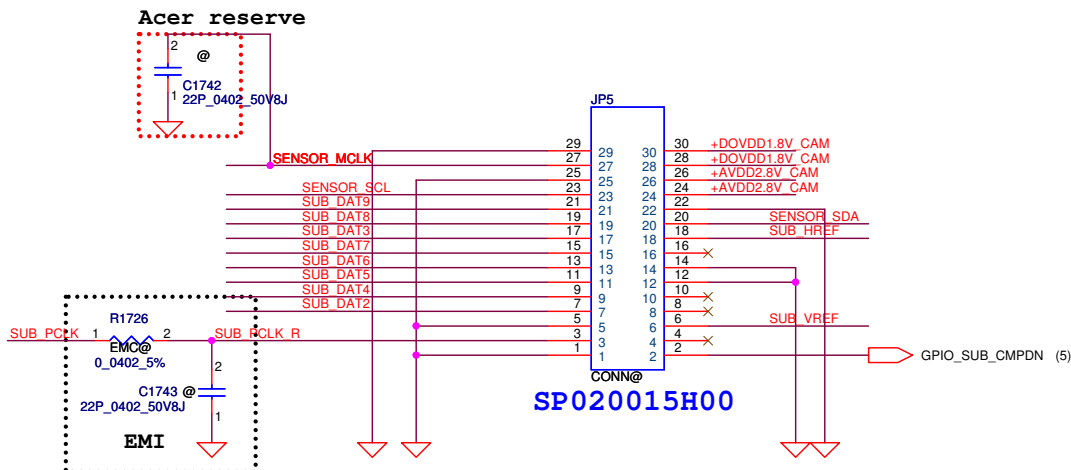
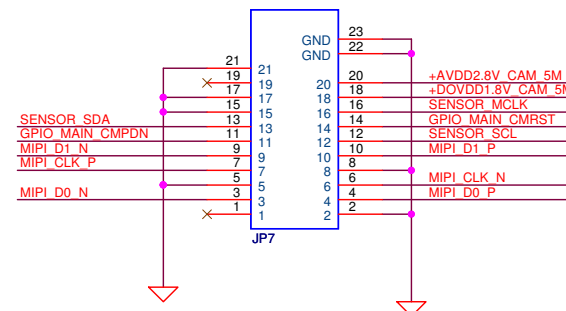
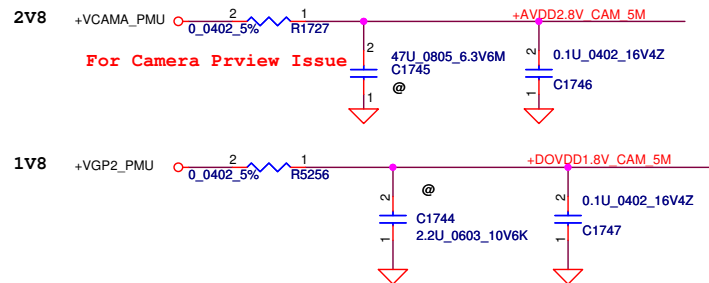
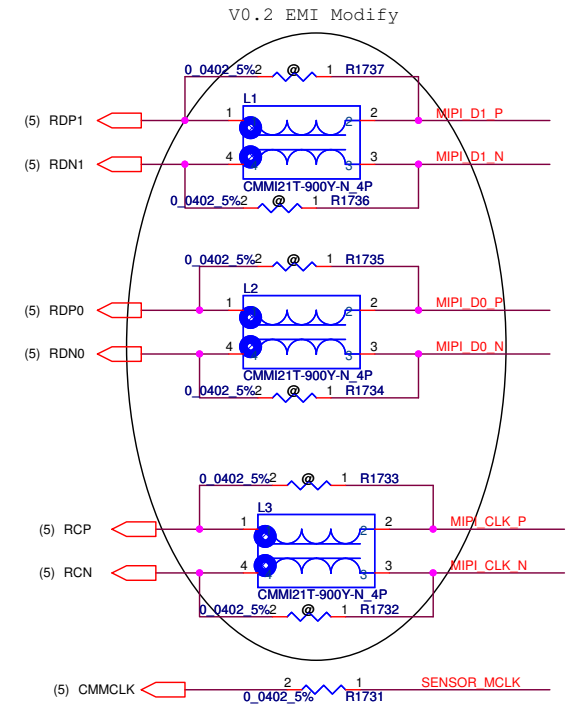
Compal GND MTK GND

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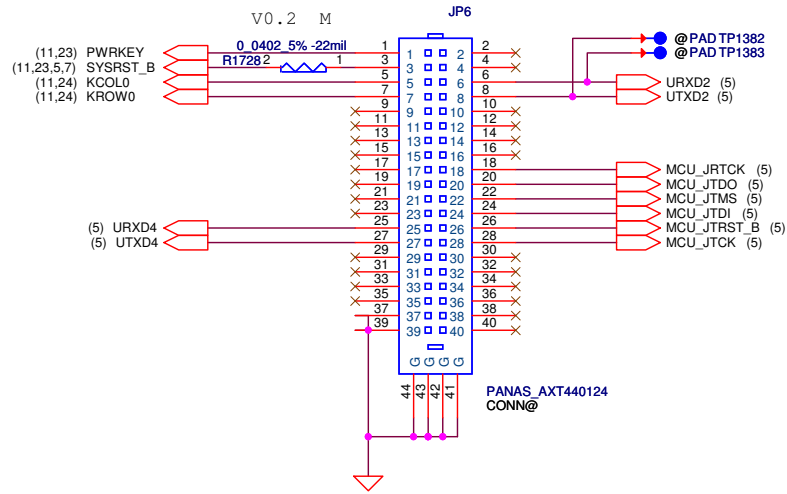
clock setting		XTEST	EEDI	ANTSEL_3	
	2.8V TCXO or OSC	0	0	0	Default
	1.8V TCXO or OSC	0	1	0	
	XTAL	0	0	1	
	external clock mode	0	1	1	
WIFI host interface		XTEST	ANTSEL_2	ANTSEL_1	
	WIFI :SDIO1	0	0	0	Default
	WIFI :SDIO2	0	0	1	
	WIFI :SPI	0	1	0	
	WIFI :reserved	0	1	1	
BT/common host interface		XTEST	ANTSEL_0		
	UART1	0	0		Default
	SDIO2	0	1		

5M Camera

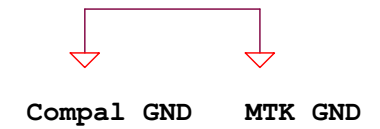
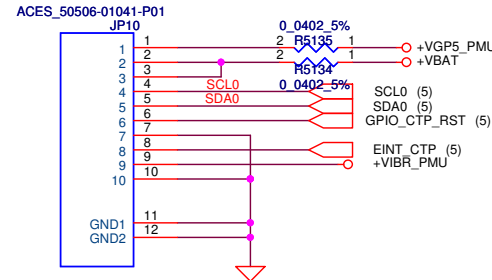


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Common Debug

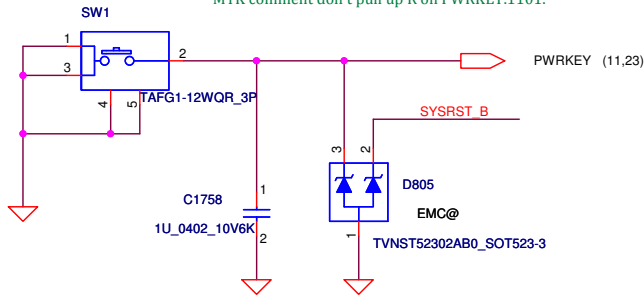


Touch

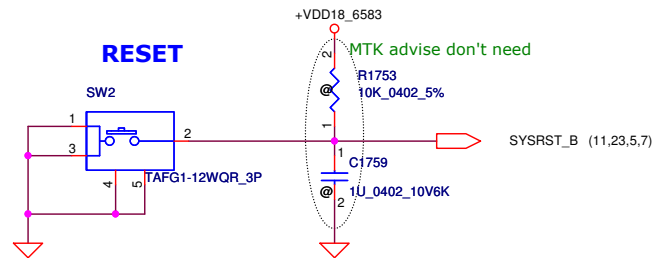


Power-on Button

MTK comment don't pull up R on PWRKEY.1101.



RESET

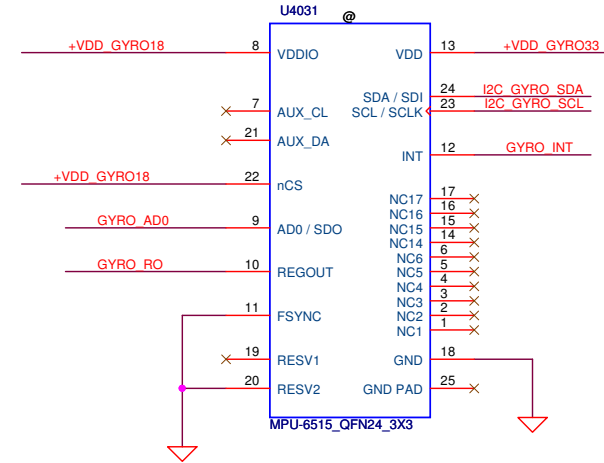
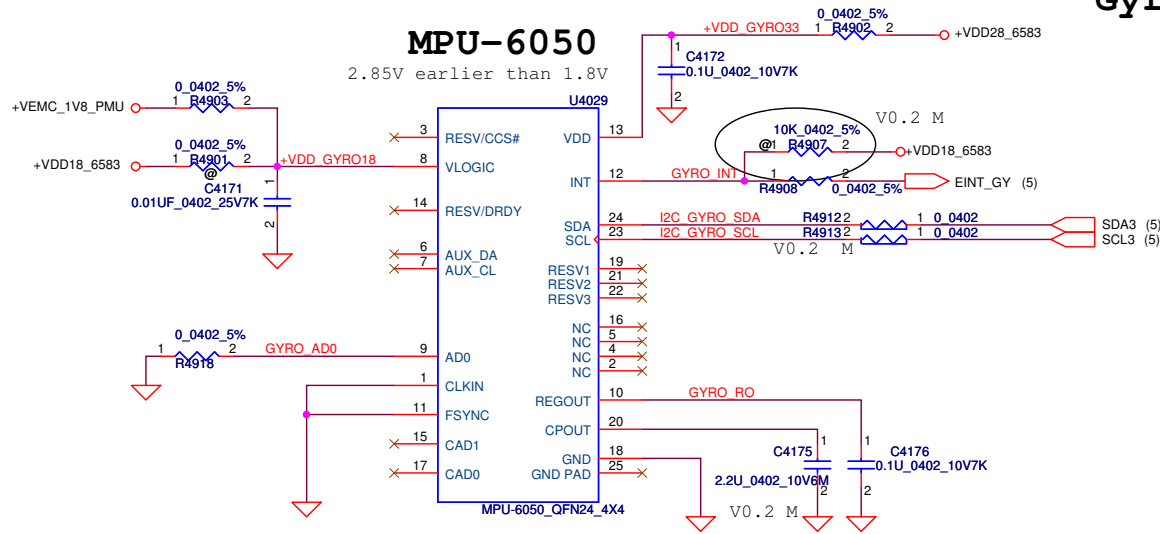


Gyro G-Sensor

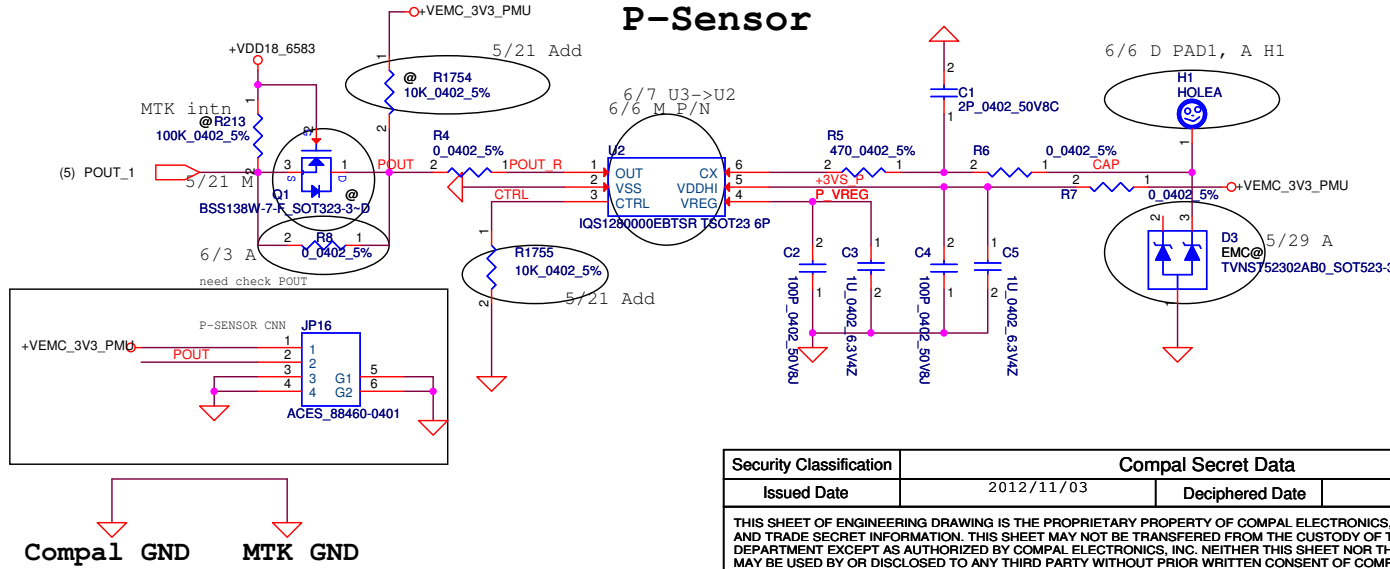
MPU-6515

MPU-6050

2.85V earlier than 1.8V



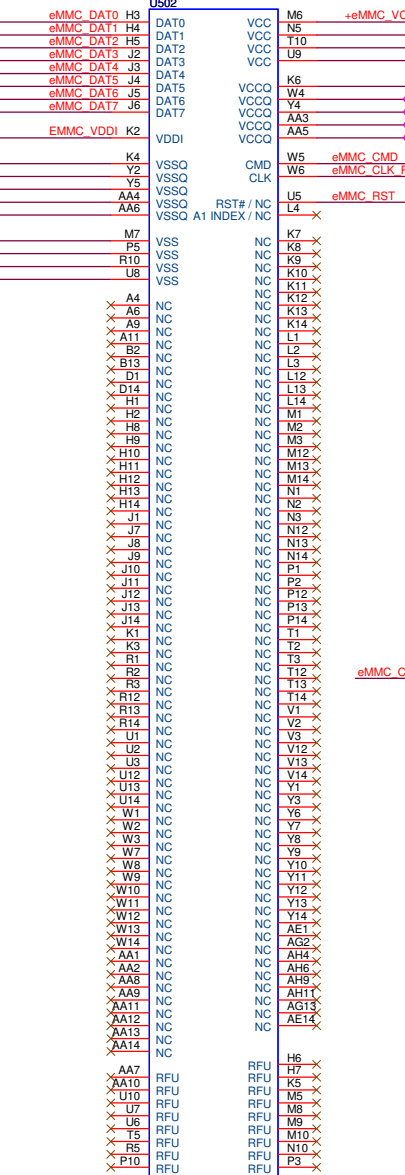
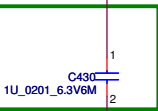
P-Sensor



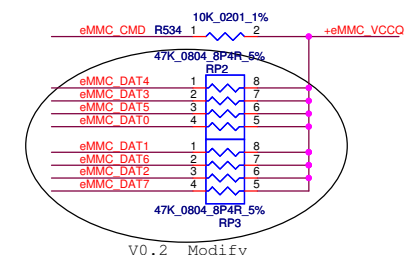
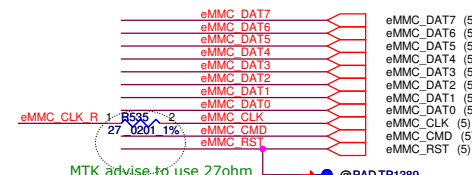
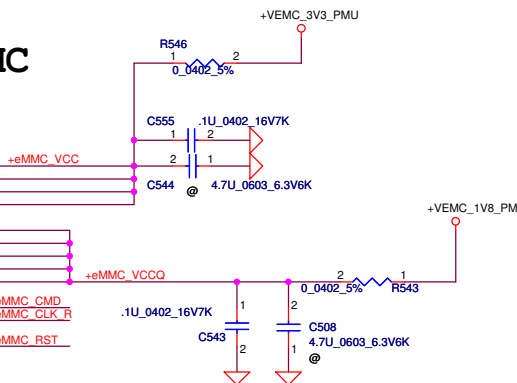
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169 ball eMMC

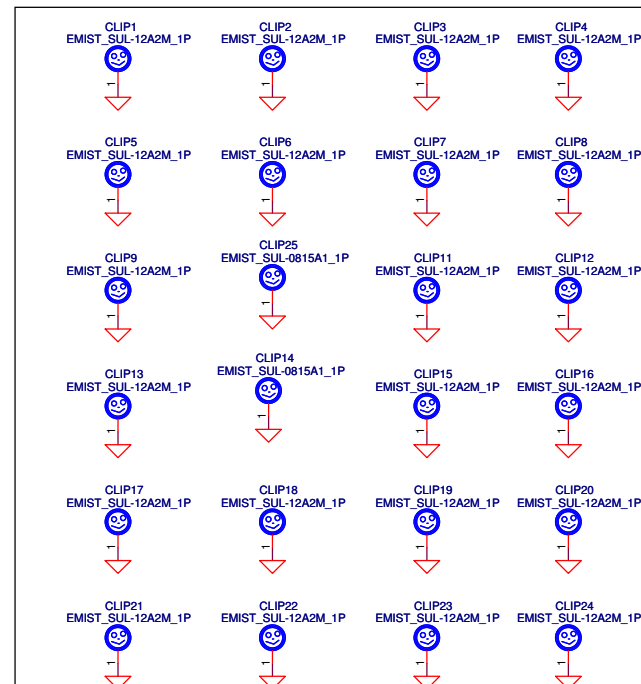
Close to Memory



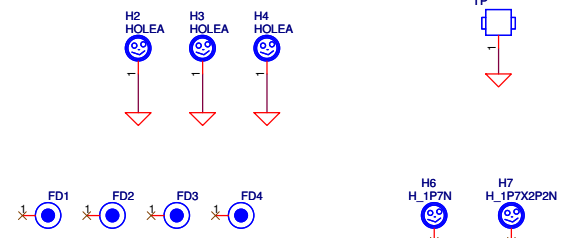
SDIN4E2-16G-T_TFBGA_169P-P
@compal footprint



- U502 KIN 8GB@
SA00006MF30
Kingston 8G KE4CN3K6A
- U502 KIN 16GB@
SA00006MG30
Kingston 16G KE4CN4K6A
- U502 HYN 8GB@
SA00006PW10
HYNIX 8G H26M42002GMR
- U502 HYN 16GB@
SA00006VJ10
HYNIX 16G H26M52002EQR
- U502 SAM 8GB@
SA00006VE10
Samsung KLM8G1WE4A-A001
- U502 SAM 16GB@
SA00006Z610
Samsung KLMAG2WE4A-A001



SCREW HOLE



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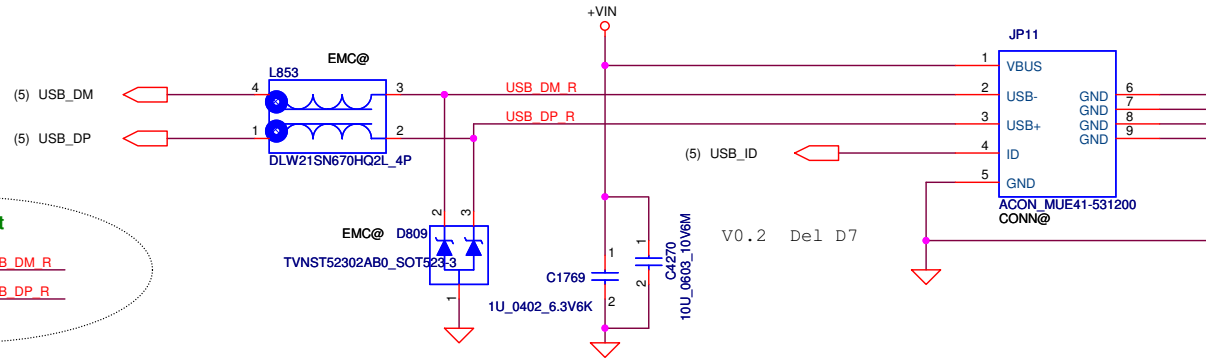
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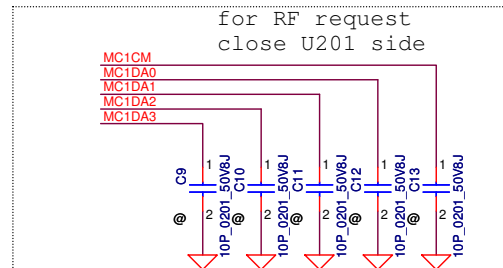
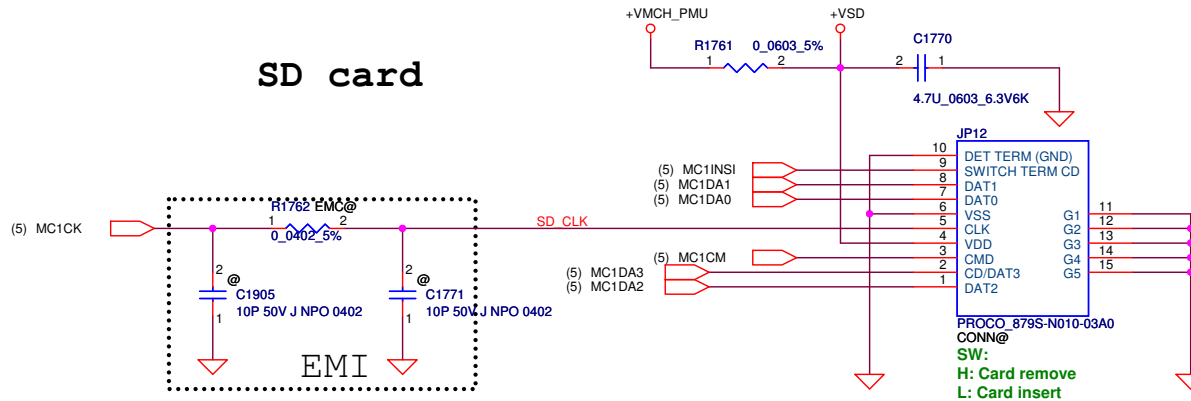
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Micro-USB

If mini-A connector insert => CID < 0V => Low
 If mini-B connector insert => CID > 1.2V => High
 IDPULLUP pin is replaced by 1.2V power source.

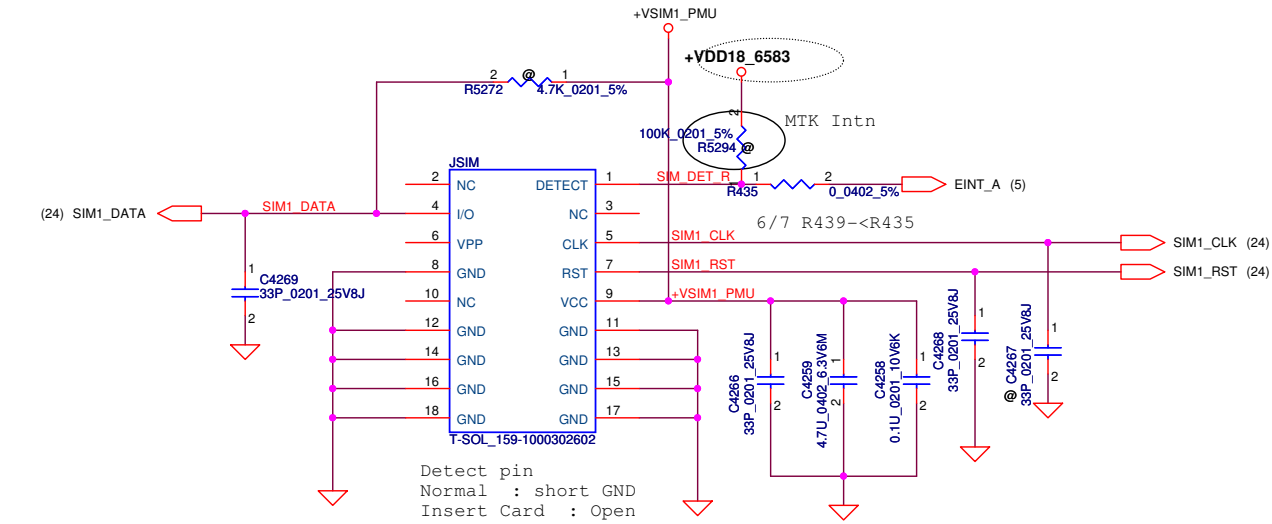


SD card



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										Connector-2(SD card/G-se)	
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SIM CARD



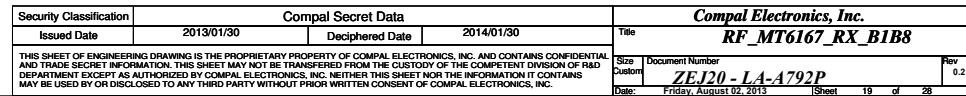
Compal GND MTK GND

V0.2 Del DM1,DM2

V0.2 Del 3G SPK & HP

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Note : Use RX Co-banding
GSM850 = 3G B5
GSM900 = 3G B8
GSM1900= 3G B2

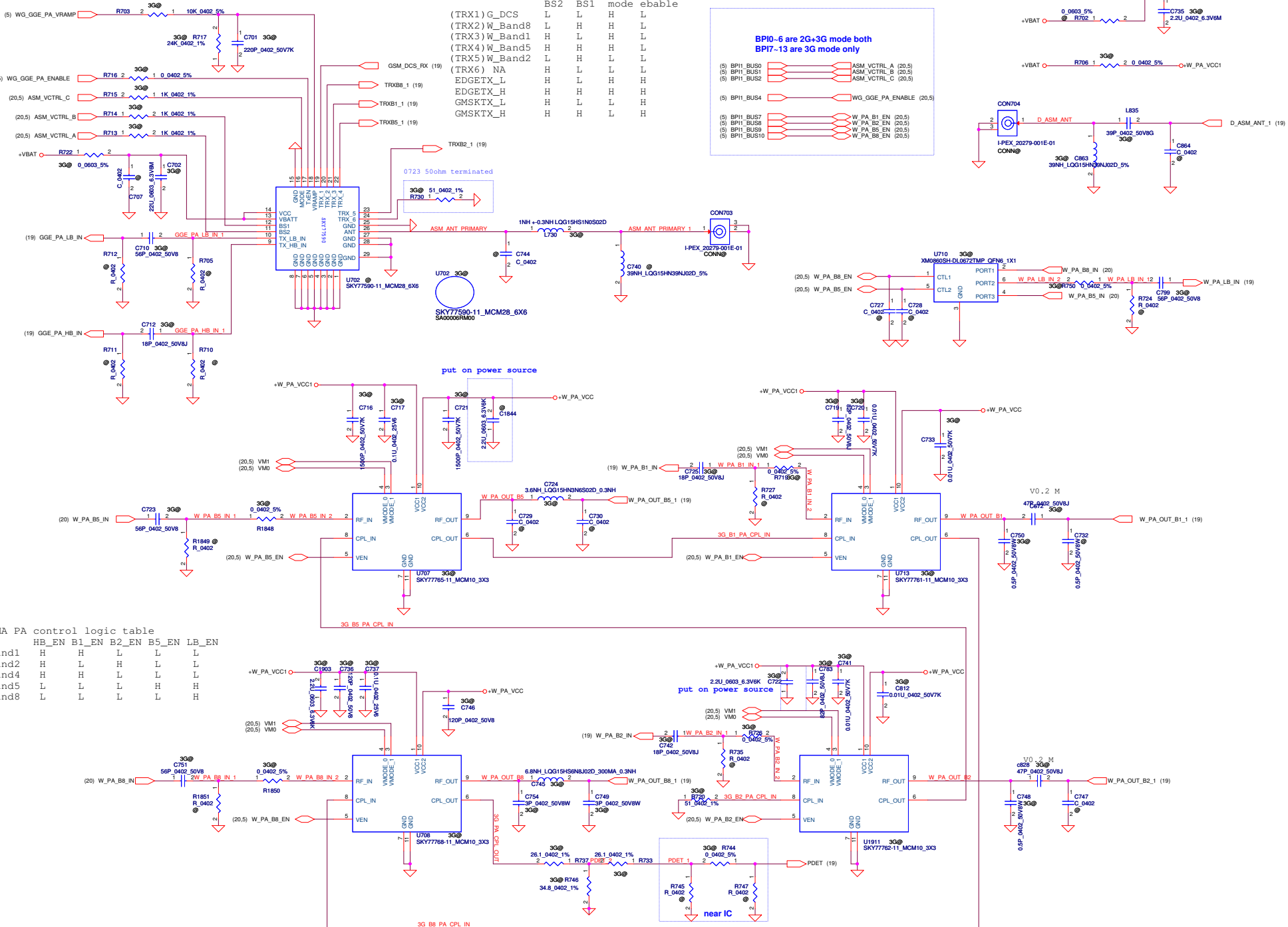


SKY77590 control logic table

	VctA	VctB	VctC	TxE
BS2	BS1	mode	enable	
(TRX1)G_DCS	L	L	H	L
(TRX2)W_Band8	L	H	H	L
(TRX3)W_Band1	H	H	H	L
(TRX4)W_Band5	H	H	H	L
(TRX5)W_Band2	L	H	L	L
(TRX6)NA	L	L	L	L
EDGE_TX_L	H	L	H	H
EDGE_TX_H	H	H	H	H
GMSK_TX_L	H	L	L	H
GMSK_TX_H	H	H	L	H

BP10-6 are 2G+3G mode both
BP17-13 are 3G mode only

(5) BP10_BUS0	ASM_VCTRL_A (20.5)
(5) BP11_BUS1	ASM_VCTRL_B (20.5)
(5) BP11_BUS2	ASM_VCTRL_C (20.5)
(5) BP11_BUS4	WG_OGE_PA_ENABLE (20.5)
(5) BP11_BUS7	W_PA_B1_EN (20.5)
(5) BP11_BUS8	W_PA_B2_EN (20.5)
(5) BP11_BUS9	W_PA_B5_EN (20.5)
(5) BP11_BUS10	W_PA_B8_EN (20.5)

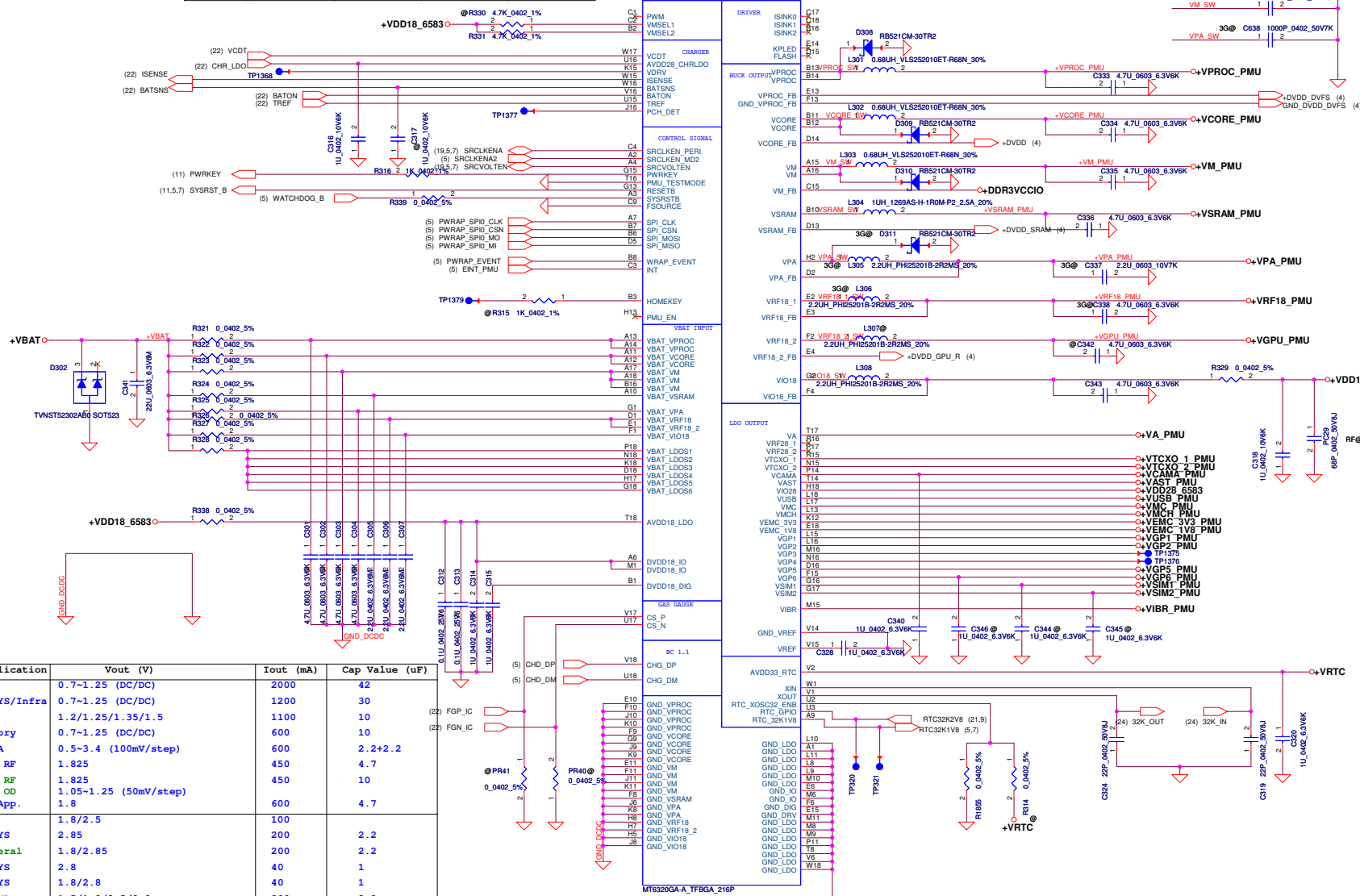


WCDMA PA control logic table

	HB_EN	B1_EN	B2_EN	B5_EN	B8_EN
W_Band1	H	H	L	L	L
W_Band2	H	L	H	L	L
W_Band4	H	H	L	L	L
W_Band5	L	L	L	H	H
W_Band8	L	L	L	L	H

PMIC

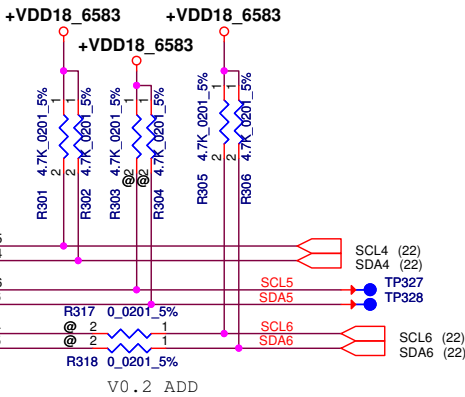
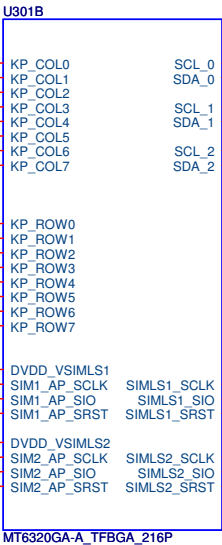
	LPDDR2/1.2V	DDR3U/1.25V	DDR3L/1.35V	DDR3/1.5V
VMSEL2	L	L	H	H
VMSEL1	L	H	L	H



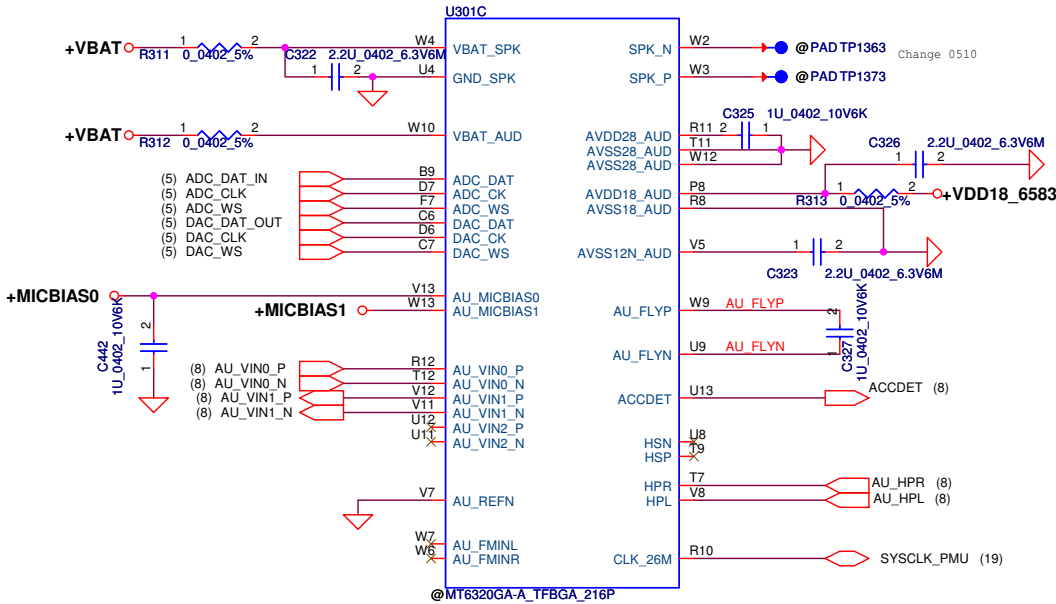
	Symbol	Application	Vout (V)	Iout (mA)	Cap Value (uF)
Buck	VPROC	CPU	0.7~1.25 (DC/DC)	2000	42
	VCORE	MDSYS/Infra	0.7~1.25 (DC/DC)	1200	30
	VM	VM	1.2/1.25/1.35/1.5	1100	10
	VSRAM	Memory	0.7~1.25 (DC/DC)	600	10
	VPA	3GPA	0.5~3.4 (100mV/step)	600	2.2+2.2
	VRF18_1	1st RF	1.825	450	4.7
	VRF18_2	2nd RF	1.825	450	10
Analog LDO	VIO18	GPU OD	1.05~1.25 (50mV/step)	600	4.7
	VA	MDSYS	1.8/2.5	100	2.2
	VRF28_1	General	2.85	200	2.2
	VRF28_2	General	1.8/2.85	200	2.2
	VTCXO_1	MDSYS	2.8	40	1
	VTCXO_2	MDSYS	1.8/2.8	40	1
	VCAMA	VCAMA	1.5/1.8/2.5/2.8	200	2.2
Digital LDO	VIO28	MT6168	2.8	400	2.2
	VAST	MT6168	0.9/1.0/1.1/1.2	300	2.2
	VUSB	T-Card	3.3	200	1
	VMC	T-Card	1.8/3.3	200	1
	VMCH	T-Card	3.0/3.3	800	4.7
	VEMC_3V3	eMMC (Core)	3.0/3.3	800	4.7
	VEMC_1V8	eMMC	1.2/1.3/1.5/1.8/2.5/2.8/3.0/3.3	200	2.2
	VGP1	VCAMD	1.2/1.3/1.5/1.8/2.5/2.8/3.0/3.3	400	2.2
	VGP2	VCAM_AF	1.2/1.3/1.5/1.8/2.5/2.8/3.0/3.3	200	1
	VGP3	CTP/CHMB	1.2/1.3/1.5/1.8/2.5/2.8/3.0/3.3	200	1
	VGP4	CTP/CHMB	1.2/1.3/1.5/1.8/2.5/2.8/3.0/3.3	200	1
	VGP5	CTP/CHMB	1.2/1.3/1.5/1.8/2.5/2.8/3.0/3.3	200	1
	VGP6	CTP/CHMB	1.2/1.3/1.5/1.8/2.5/2.8/3.0/3.3	200	1
	VSIM1	VSIM1	1.2/1.3/1.5/1.8/2.5/2.8/3.0/3.3	200	1
	VSIM2	VSIM2	1.2/1.3/1.5/1.8/2.5/2.8/3.0/3.3	200	1
Vibrator	VIBR	Vibrator	1.2/1.3/1.5/1.8/2.5/2.8/3.0/3.3	200	1
RTC	VRTC	RTC Block	2.8	2	1~22

PMIC_Audio

Digital



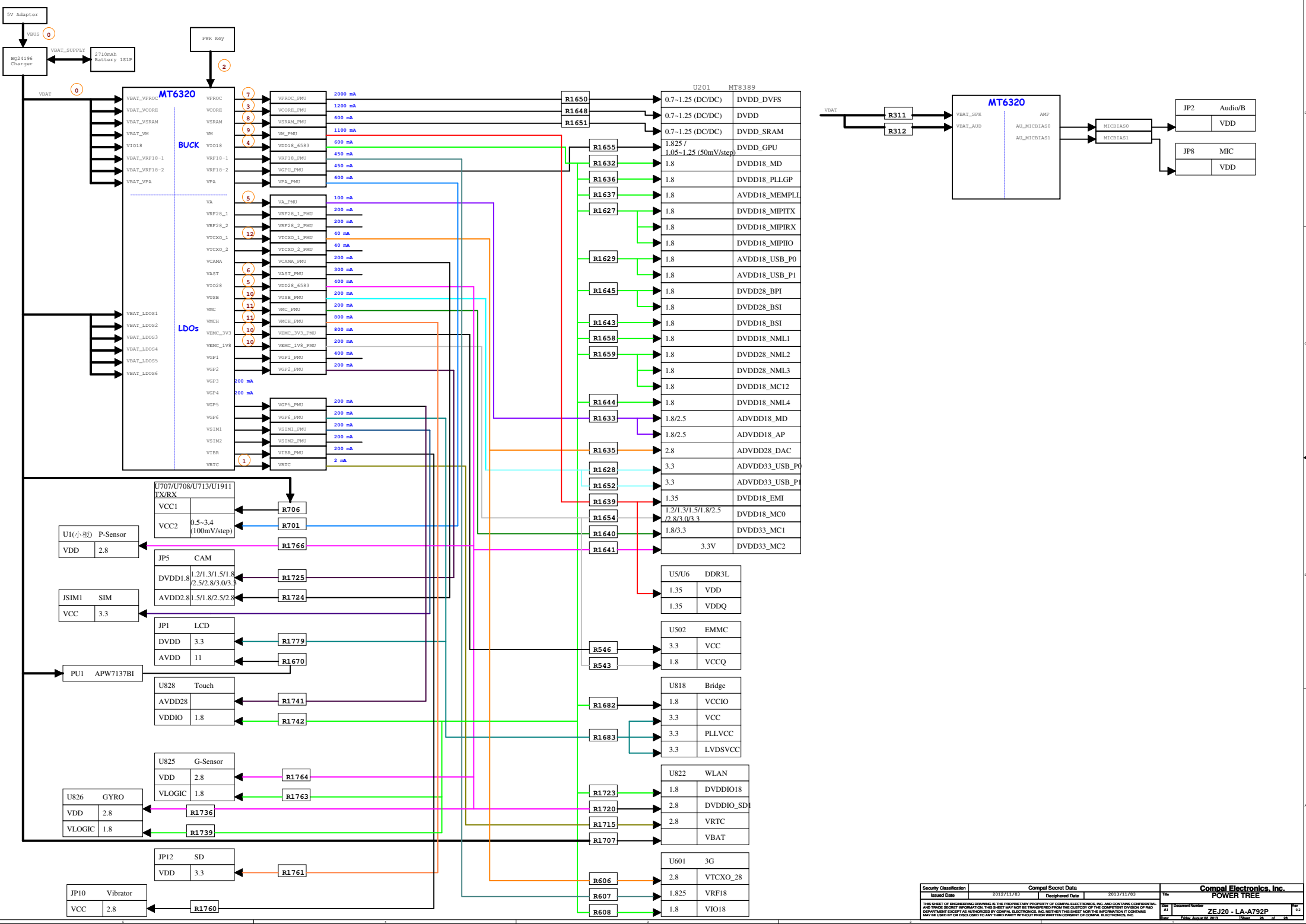
Audio



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5	4	3	2	1
D				D
C				C
B				B
A				A

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2013/3/11
Update PD11 , D308 , D309 , D310 , D311 , L301 ,
L302 , L303 , L304 , L307 , C647 , C646 , C635 ,
C638 compal P/N
Change to un-pop : PR50 , R1838 , R314 ,R315
Change to pop : R1855

2013/3/13
Add C318

2013/3/14
Del R332,R348

2013/4/1
add R1847
reserve 0-ohm for panel design

2013/4/10
reserve C346 for VGP6 PMU
PR51 change to 15K_0402_1%
PH1 change to 10K_0402_1%

2013/4/15
Add PL5 , PC143 ,PC144 for EMI request
Add PC21 , PC22 ,PC23 for RF request

2013/4/22
Change L307 and C342 to reserve

2013/5/6
Change L306 and C338 BOM structure to 3G@

2013/5/6
Change PC21,PC22 and PC23 BOM structure to 3G@
PC21 change from 22P to 10P
PC22 and PC23 change 68P to 33P

2013/5/8
Change L305 and C337 BOM structure to 3G@

2013/5/8
Change D311 and C638 BOM structure to 3G@

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ZEJ20 V0.2	page	state	description
2013 08/01	P4	A	RF=> Add C1677,C1679,C1681 68P
		A	RF=> Add C4271~C4277 68P
	P5	M	R210,R212,R217,R218 Change to PR1
		A	EMI=> Add C208 0.1u
		A	Add GPIO_SW1 net
	P6	D	Del TP
		D	EMI=>Del D814
	P7	D	RF=>Del TP1394
		D	Del R5154
		M	R5187,R5190,R5191,R5193,R5197, R5220,R5222,R5223 change to short pad
		A	Add U3
		A	Add C1420,C1460,R1269,R1270
	P8	M	R1267 change to short pad
		M	EMI=> R1732~R1737 change to Short PAD
	P9	M	R1714,R1720 change to short pad
		M	R1728 change to short pad
	P11	M	R1728 change to short pad
	P12	M	R4907 NU
		M	R4912,R4913 change to short pad
	P13	M	R527~R232,R536 Change to PR2,RPR3
	P17	D	EMI=> Del D7
	P18	D	EMI=> Del DM1,DM2
		D	Del 3G SPK & HP
	P19	M	RF => C676 1.5nH ,C652 1.2pF ,C617 1pF
	P20	M	RF=> C726,C828 47P
	P24	A	R317,R318,R319,R320

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